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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,576	09/20/2006	Kiyoshi Kato	0756-7833	1445

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EXAMINER	
NGUYEN, VIET Q	
ART UNIT	PAPER NUMBER
2827	

MAIL DATE	DELIVERY MODE
09/09/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,576	KATO ET AL.	
	Examiner	Art Unit	
	Viet Q. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *THREE* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Pre-amendment filed on 9/20/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,3 and 14* is/are allowed.

6)☒ Claim(s) *1,4-7,11-13,15-18 and 22* is/are rejected.

7)☒ Claim(s) *8-10, 19-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The pre-amendment filed on **9/20/2006** has been entered, and claims **1-22** are present for examination. This action replaces that last Office Action, which was erroneous and defective.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1, 4-7, 11-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Shimizu et al (US 6,097,622)** in view of **either Ovshinsky et al (US 5,296,716) or Klersy et al (US 5,536,947).**

Shimizu et al (see fig. 37A) clearly shows a semiconductor device using a detector/transmitter circuit for receiving/transmitting electromagnetic waves from an antenna (88, see col. 13, lines 50-65), and a diode-rectifier circuit 9633) as claimed "power supply circuit" for generating a power supply voltage (DC 5V)from said carrier wave of the electromagnetic wave/input signals, and also shows the use of a non-volatile memory array (611, 612) which also includes a plurality of word lines

intersecting with plurality of bit lines (in both 1st & 2nd directions, see Fig. 9). Furthermore, Fig. 46(a-c) also show in detail how the antenna (114) can be used to send power and command data (115) to the carrier (117) and receives data (116) to same carrier (117), and a carrier (119, Fig. 46c) has a FRAM (Ferroeletric Random Access Memory) for storing such data received from the antenna. See also col. 7, lines 30-45 description.

Although the patent does not specifically specify the word "phase change" for such memory, it would still have been obvious and/or expedient knowledge to one having ordinary skill in this art that any ferroelectric material has two changeable phases and thus can be programmed to store two distinct memory states, and therefore meet the claimed limitation of "phase change memory" as well. Furthermore, in view of other prior arts which have already disclosed that all phase change materials have either amorphous or crystalline states as their main memory states, it would have been obvious to one having ordinary skill in this art to easily create such a multi-state memory structure. For example, see Ovshinsky et al (col. 7-9) and Klersy et al (see col. 9-12) at least suggested these memory states for various combinations of these phase change materials, etc.

Regarding other claimed features, Fig. 47 shows the use of modulation and demodulation circuit (FSK 58) besides other interface and/or clock circuits, and the patent also suggests the use flexible substrate mountable on circuit carrier and embeddable as for small ID tags applications, etc..

4. Claims **1, 4-7, 11-12** are rejected under 103 over either **Hazama (US 6,234,902)** in view of **either Ovshinsky et al (US 5,296,716) or Klersy et al (US 5,536,947).**

Hamaza (see fig. 5) clearly shows a semiconductor device using a RF detector/transmitter circuit (2) for receiving/transmitting radio frequency signals from the antenna 2 (see also col. 8-10 description), and a power supply circuit (104) for generating an internal power supply voltage from said carrier wave of the electromagnetic wave/input signals (20), and also shows the use of a non-volatile memory array (110, 111) which also includes a plurality of word lines intersecting with plurality of bit lines. Furthermore, col. 26 mentions that such memory is multi-valued and can be made of FRAM (Ferroelectric random Access memory) type as well.

Although the patent does not specifically specify the word "phase change" for such memory, it would still have been obvious and/or expedient knowledge to one having ordinary skill in this art that any ferroelectric material has two changeable phases and thus can be programmed to store two distinct memory states, and therefore meet the claimed limitation of "phase change memory" as well. Furthermore, in view of other prior arts which have already disclosed that all phase change materials have either amorphous or crystalline states as their main memory states, it would have been obvious to one having ordinary skill in this art to easily create such a multi-state memory structure. For example, see Ovshinsky et al (col. 7-9) and Klersy et al (see col. 9-12) at least suggested these memory states for various combinations of these phase change materials, etc.

Regarding other claimed features, Fig. 5 also shows the use of modulation and

demodulation circuit (107, 108) besides other interface and/or clock circuits, and the patent also suggests the use flexible substrate mountable on circuit carrier and embeddable as for small ID tags applications, etc.

5. Claims **13, 15-18 & 22** are rejected under 103 over **Shimizu et al (US 6,097,622) or Hazama (US 6,234,902)** in view of either **Ovshinsky et al (US 5,296,716)** or **Klersy et al (US 5,536,947),** as discussed above, and in further view of **Tomon (US 6,727,862).**

Regarding claims **13, 15-18 & 22**, **Shimizu et al (see Fig. 37A) or Hazama (see Fig. 5)** in view of either **Ovshinsky et al (col. 7-9)** or **Klersy et al (col. 9-12)** have been discussed above to teach every essential recited elements except for the use of thin film transistor.

Claims **13 & 15** add the limitation or the use of a thin-film transistor which is not seen nor suggested in the primary references above. However, Tomon et al (see col. 3) suggests the use of a very thin film substrate (10 micro-meters) and a thin-film, bare IC control circuit of 40 micro-meter thickness for use in a similar memory structure that includes antenna, power supply circuit and memory circuit, etc., but Fig. 6 further shows the inside structure of control circuit (bare IC 2) which could include other FET transistors (not shown) as obvious control thin film transistors as their design choices without further modification or hindsight construction.

6. Other claims are either allowed or objected as being dependent upon rejected claims, but contain allowable subject matter as prior arts fail to teach or fairly suggest other claimed features such as, i.e., light transmitting bit lines, or thin film transistor used on a glass substrate, or glass substrate, or specific phase change materials, and/or combinations of these materials making up the phase change memory, etc.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Viet Q Nguyen/
Primary Examiner, Art Unit 2827

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Primary Examiner
Art Unit 2827

V. Nguyen
6/9/2208